

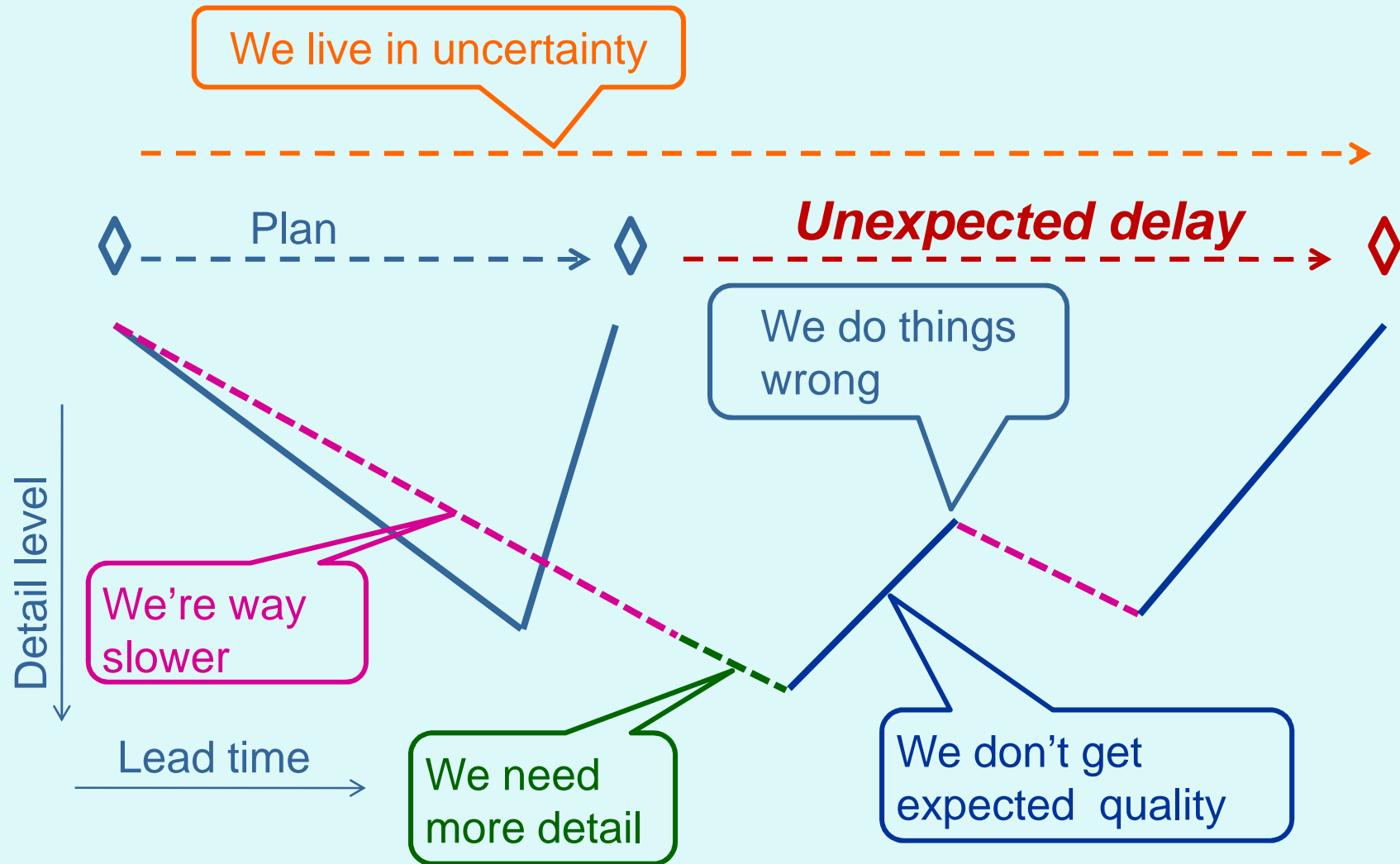
Wings



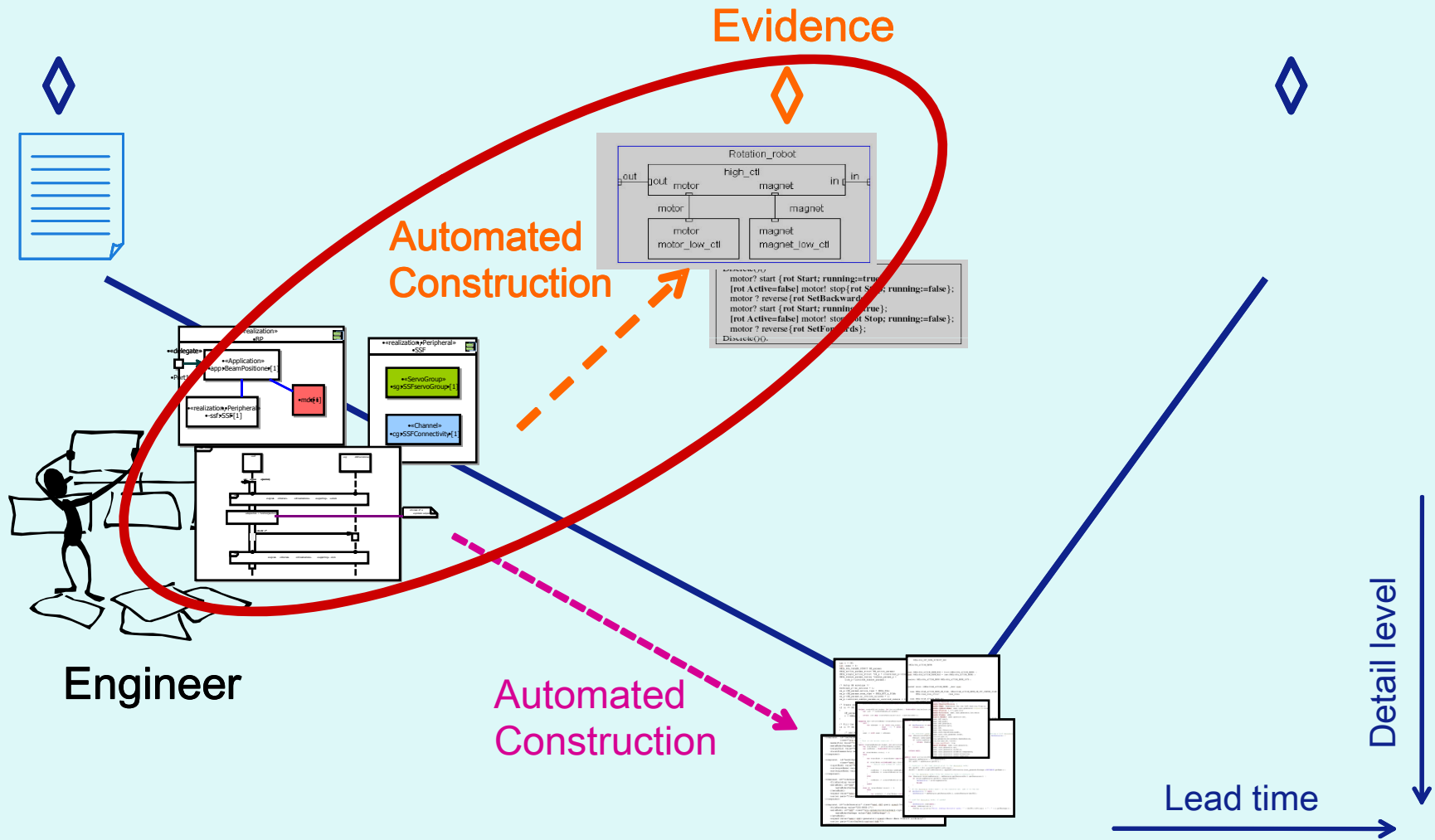
Predicting Timing Performance of Wafer Scanners

Jeroen Voeten, Teun Hendriks, Bart Theelen, Jan Schuddemat (ESI)
Wouter Tabingh Suermondt, John Gemei, Kees Kotterink, Dick de Reus, Cees van Huët (ASML)
KWR09127

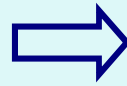
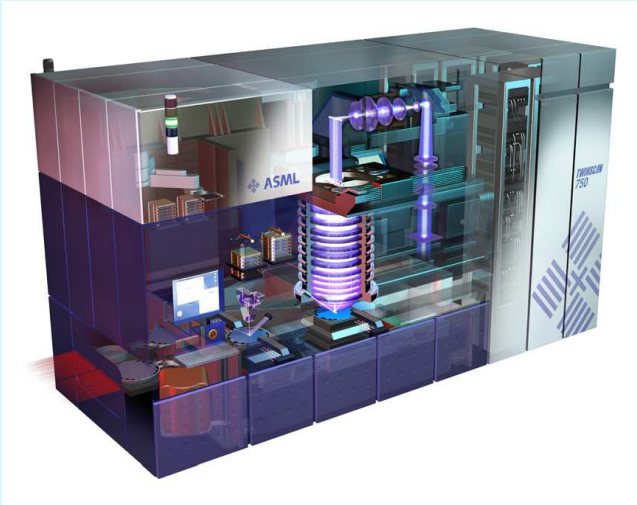
The V-model: Current practice



Context in the MDE approach

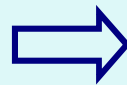
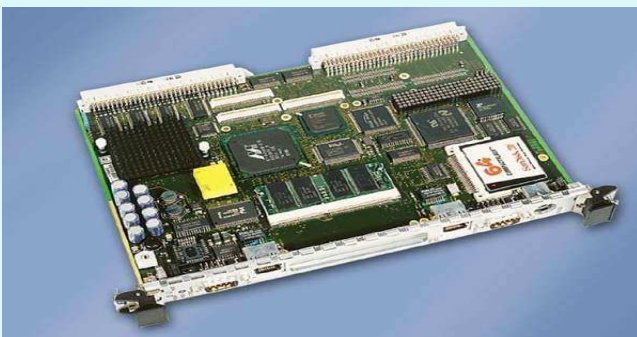


Embedded control systems trends



Embedded control applications

- Increasing functionality
- Increased number of dependencies
- Increasing timing requirements



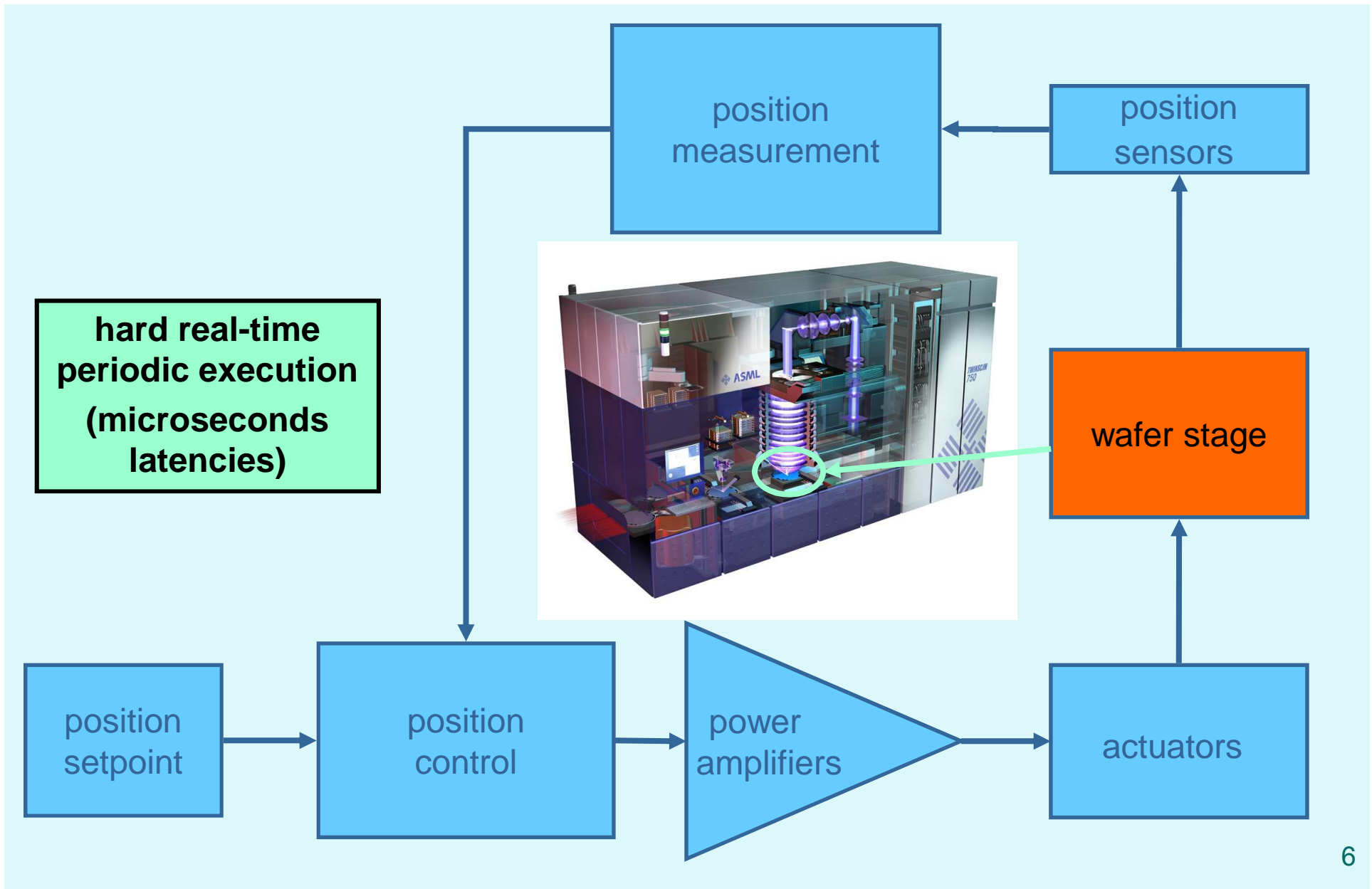
GP execution platforms

- Free performance lunch is over
- Unpredictable timing performance

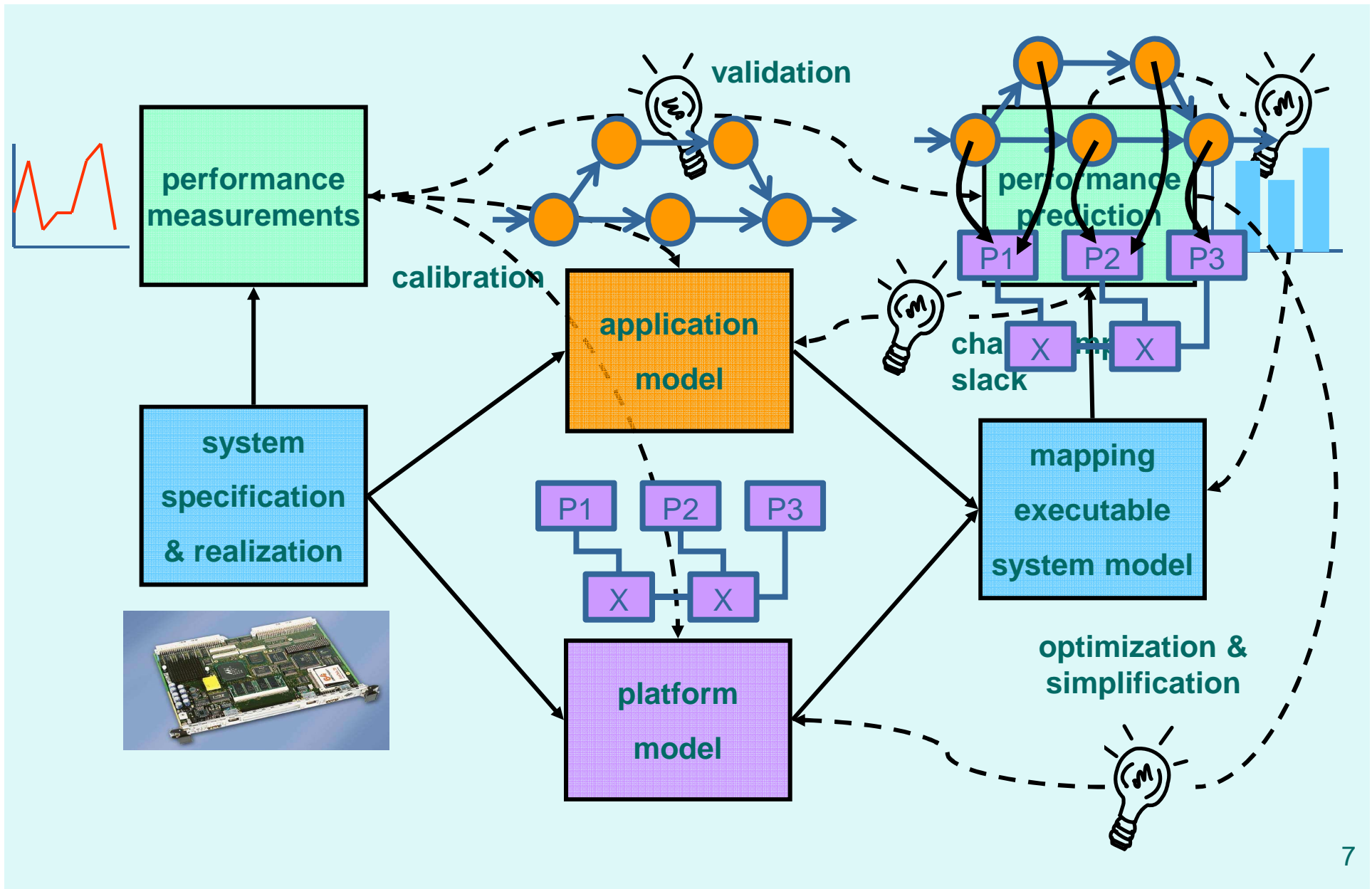
Performance modeling goals

- **Systematic way-of-working to predict and optimize timing performance**
 - Early feedback about impact of design decisions on timing performance
 - Cheap investigation of alternatives
- **Prevent rework to resolve timing performance problems encountered during system integration**
- **Anticipate the future**
 - Roadmap development for critical embedded subsystems to prevent performance issues in the future

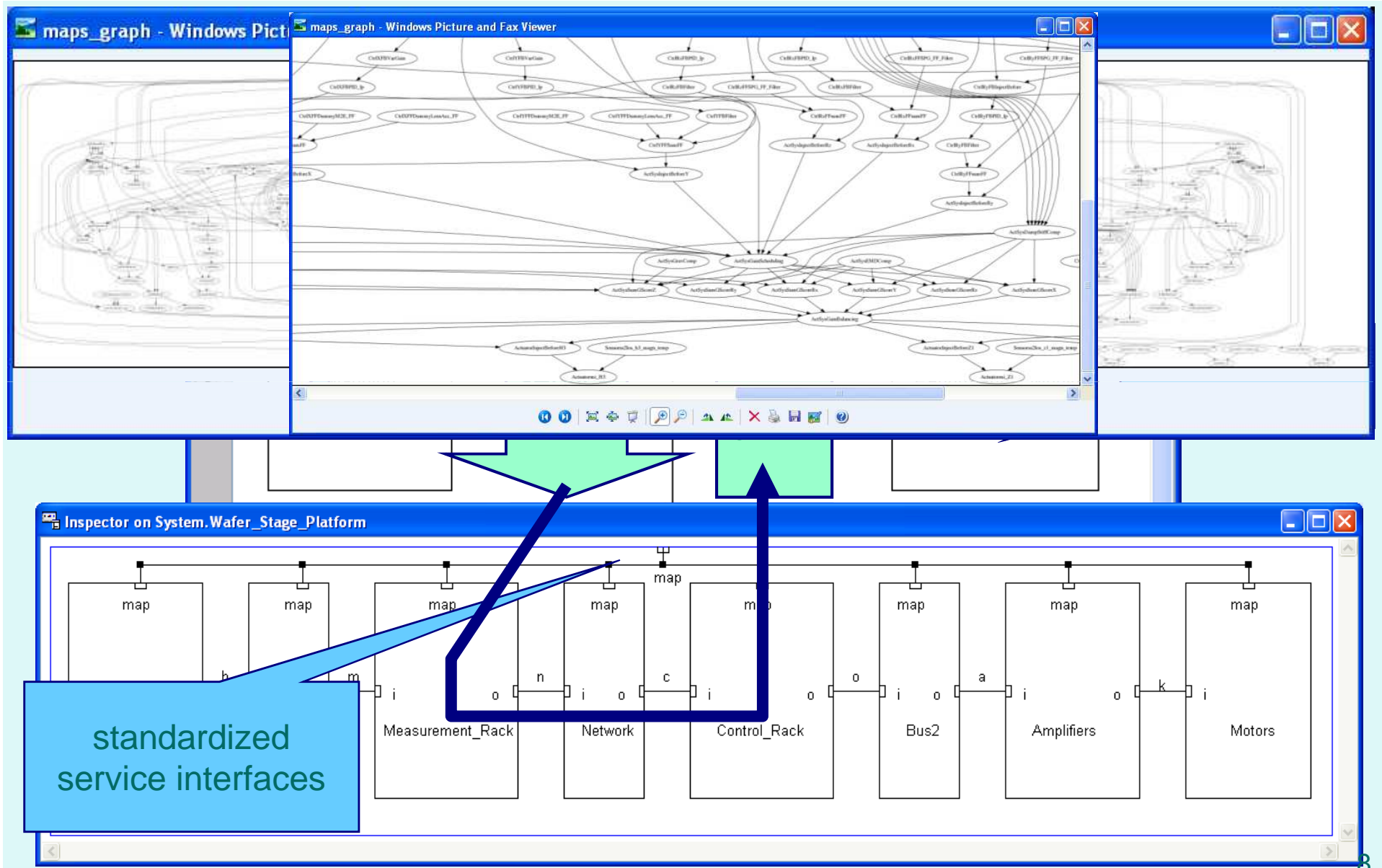
Wafer stage control



Modeling Approach: Y-charting



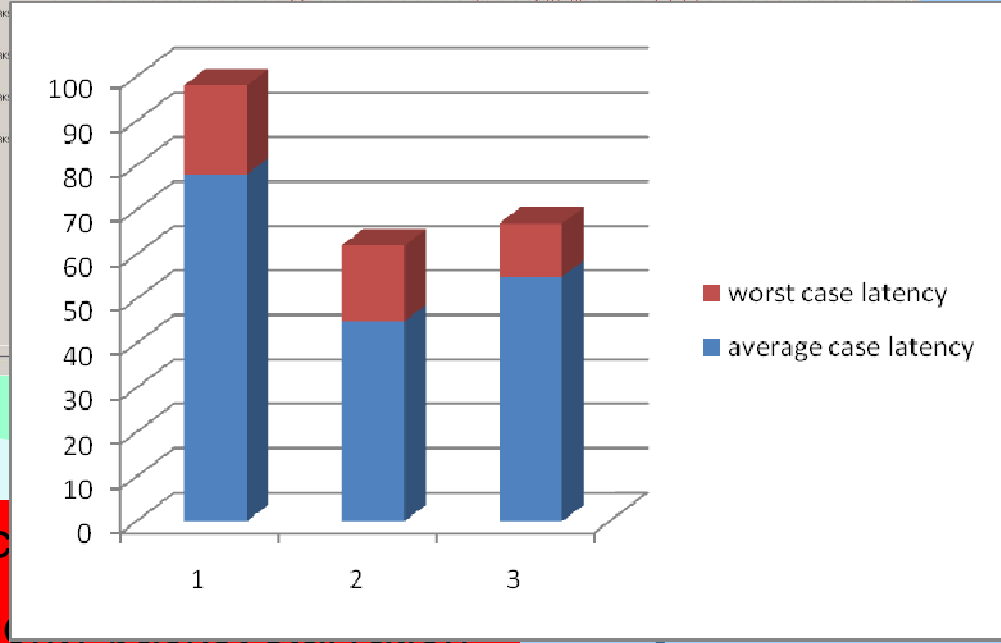
Wafer stage control: executable model



Formalism: POOSL

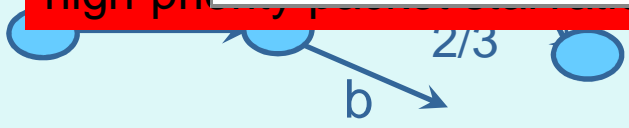
```

handleInputPort2() | p:RIOPacket |
  ip2?packet(p | scheduler inputQueueAccepts(2,p));
  scheduler setOutputPortFor(p);
  par
    if storeAndForwardMode then delay switchLatency
    else delay switchLatency
  fi;
  scheduler inputQueuePut(2,p)
  and
  handleInputPort2()
  rap.
  
```



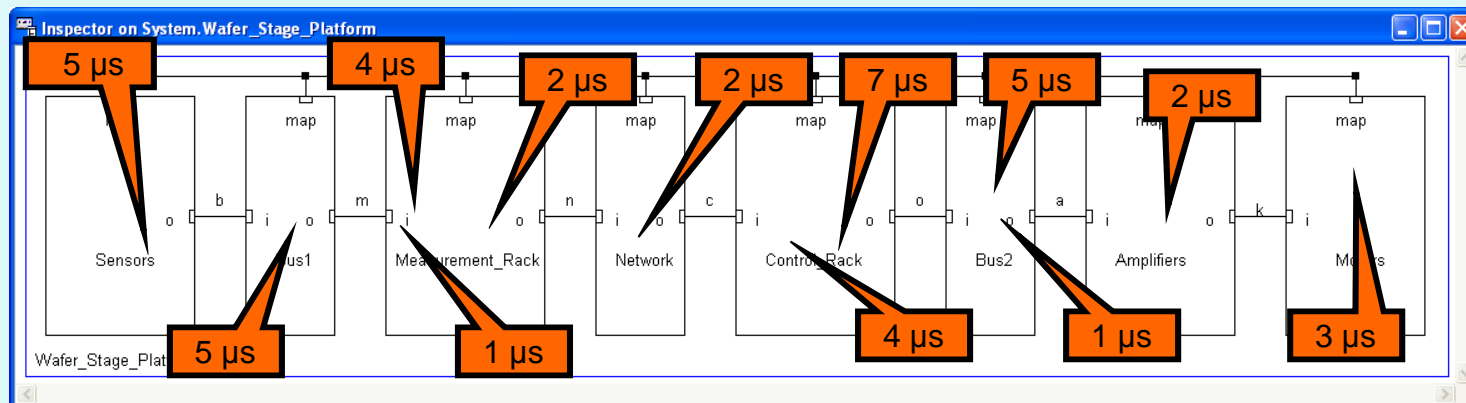
correctness verification

deadlock
high-pri



Industrial results

- Modeling method to predict and optimize timing performance
- Dissemination
 - workshops
 - ASML is taking up results in various projects
 - embedded software, digital hardware, mechatronics
- Optimizations
 - 16 different improvements identified
 - over 50% performance gain
 - determination of platform limits

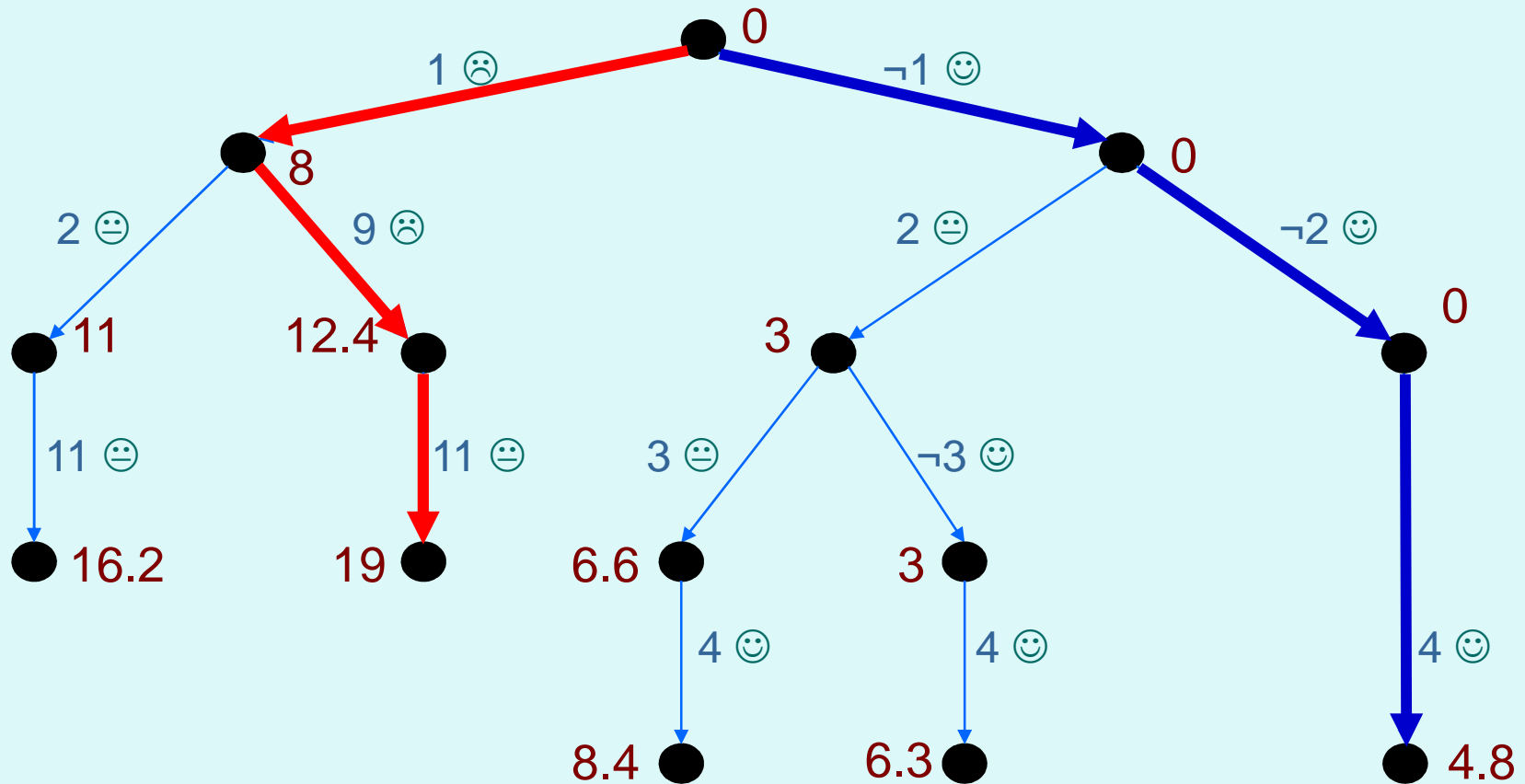


Industrial results

- Improvement roadmap

- cost/risk analysis
- decision trees

short term roadmap
mid term roadmap



Industrial results: scaling up

Engineering world

Large number of multi-disciplinary design files / formats

Embedded System Construction (design)



automated construction

Modeling world

Structure domain in DSL's

application model

mapping
Laborious exercise

platform model

automated construction



executable system model

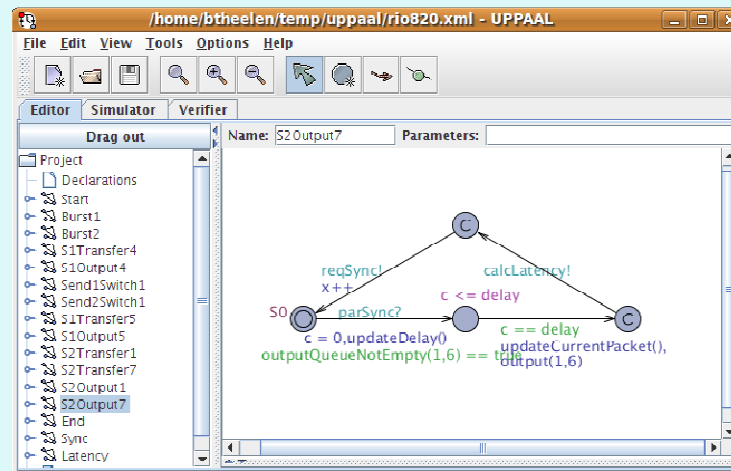
Multiple interacting subsystems
(4000 tasks, 250 sensors/actuators
14000 dependencies)

Outlook: starting point for construction as well

- **Model architecture**
 - respect Y-chart modularization
 - interface standardization
- **Successful application to complex industrial system**
 - fast model construction with team of specialists
 - fast model adaptability to analyze alternatives
 - model component reuse
 - automated model construction through DSLs

Scientific results (cont'd)

- **Scalable simulation-based analysis**
 - 5000 concurrent processes
 - 30 iterations per minute
- **Exhaustive analysis**
 - small part of system
 - Quasimodo, FP7 (FMT group, Twente)
 - modular timed automata specifications



Challenge: very-high performance control

- **From rigid to non-rigid body control**
- **Improve control Bandwidth with order of magnitude**
 - higher sample frequencies
 - lower latencies
- **Required innovation: centralized \Rightarrow distributed control**
 - exploit application-level concurrency
 - improve execution times of application tasks
 - general-purpose \Rightarrow dedicated embedded architectures
 - distributed mechatronic control

The V-model: The MDE way

